# VHDL by Example, errata

We now introduce a few common state-type operations to show how increasingly sophisticated register-based functions are implemented in process statements. A four-bit counter is enabled by a "start" event, and stopped by a "stop" event. The SR flop allows the start and stop events to be short, e.g. one-clock pulses, rather than a continuously enabling flag. Additionally, for further illustration, we delay the ~~start~~ stop signal two clocks and provide it as an output.

You'll notice that we have not shown the asynchronous reset in the diagram. This is done for clarity; from this point forward it is assumed. It is implemented in the code, and always will be (in this book).